4.1.2 InAs nanowire circuits fabricated by field-assisted self-assembly on a host substrate

Student: R. Richter
Scientist: K. Blekker, O. Benner
in collaboration with: T. Waho (Sophia University, Tokyo, Japan)

Introduction

Today, nanowire devices are referred to as a qualified successor of CMOS electronics. Both a performance superior to silicon (Si) MOSFETs and a rational, cost-efficient technique to implement multiple nanowire devices into circuits are recommended. We propose to transfer the nanowires from a growth substrate onto a carrier or host substrate using field-assisted self-assembly. This approach allows for the implementation of epitaxial nanowire independent of the choice of growth substrate and its crystal orientation. It avoids any constraints of high qualitative nanowire growth which the process needs and limitations of circuit fabrication.

In this paper we present the heterogeneous integration of InAs nanowire FET as superior performance key devices into existing patterns or circuits. The electric field applied to the pre-patterned electrodes causes a dipole moment within the nanowires which moves and aligns the nanowires to the regions of the highest field strength located between the electrodes [1]. Using this so called field-assisted self-assembly (FASA) there is no limitation in the choice of orientation or distribution across the substrate which makes this approach very interesting for heterogeneous integration into any microelectronic and nanoelectronic circuits including Si CMOS.

With optical and electron beam lithography nanowire transistors are fabricated and heterogeneously integrated into circuits. Both, inverter and sample & hold circuits are realized. The fabricated circuits are electrically characterized and simulated with Advanced Design System (ADS).

Experimental

The InAs NWs were synthesized in a metal-organic vapor phase epitaxy using the vapor-liquid-solid growth mode on GaAs(111)B or InAs(111)B growth substrate. The grown 12 µm long InAs nanowires with 50 nm diameter were mechanically transferred into isopropyl alcohol. The nanowire solution was dropped on a host substrate with various pre-patterned electrodes of 15 nm titanium (Ti) (cf. Fig. 1a-b). In order to assemble the nanowires by FASA a sinusoidal voltage with 10 V peak-to-peak and a frequency of 10 kHz was applied to the electrode pairs for two minutes. After assembling the nanowires, the interconnects between the FASA electrodes were removed by means of wet chemical etching. Next, the ohmic contacts of Ti and Au were patterned followed by room temperature deposition of 25 nm silicon nitride (SiNₓ) gate dielectric. Finally, omega-shaped top-gates of about 1 µm length were formed of Ti and Au. High-speed measurements are performed on wafer using G-S-G probes. For the clock signal a square wave voltage with a frequency $f_{CLK} = 5f_{IN}$ is used. The output signal is measured with active probes in order to avoid a short cut due to the 50 Ohms characteristic impedance of the high-speed measurement set-up. This active probe needle
contains, in addition to the RC network, an active amplifier, thus the measured signal is decoupled from the DUT.

Inverter Circuit

Fig. 1(a-c) shows a SEM micrographs of the fabricated inverter circuit using depletion-mode InAs NWFEF. The active load was realized with a gate-source short-circuited \((V_{GS} = 0 \text{ V})\) NWFEF (cf. fig. 1 (b)). In Fig. 1d the static transfer characteristic for an input voltage \(V_{IN}\) at a supply voltage \(V_{DD} = 1 \text{ V}\) is given. The output voltage \(V_{OUT}\) of an inverter should be as close as possible to 0 V in low state and to \(V_{DD}\) in high state, respectively. The latter is achieved almost perfectly pointing out a sufficiently high off-resistance of the drive transistor. A small signal gain of up to about 5 was achieved. Figure 1e shows the dynamic characteristics of one of the fabricated inverters for a square-wave input signal at a frequency of 20 MHz. The output signal was corrected for the attenuation and phase shift of the setup including the active probe identified by measurements using a “through” test element. An adapted EEMOS M1 model was used to represent the drive and load transistor with respect to their wire number and the corresponding scaling of current and small signal parameters. The effect of the capacitive load on the time constant and the asymmetric frequency response are in good agreement with the presented results.
For detailed understanding of the experimental results, the electronic circuits were simulated using the simulation software Advanced Design System (ADS) from Agilent. In a first step a MOSFET model was adapted using NWFET measurement results. Figure 2a shows the adapted transfer characteristic of the MOSFET model as well as the simulation results of the inverter circuit. The simulation results show good agreement with the measured curves. The measured absorption of the inverter circuit is higher than the absorption in the simulation (fig. 2b). This difference can be caused by the measurement setup and parasitic capacities, which are not included in the simulation. In fig. 3c) an oscilloscope with 1 MΩ input resistance was used to simulate the inverter circuit. The output signal has a much larger amplitude than previously, the absorption is only 8 decibels. Therefore, one can assume that a large part of the absorption is due to the poor 50 Ω adaptation.

![Graph showing adapted transfer characteristic of the nanowire MISFET and simulation results of the inverter circuit measured with an oscilloscope with 1 MΩ input resistance](image)

**Fig. 2**  
(a) adapted transfer characteristic of the nanowire MISFET, and (b) simulation results of the inverter circuit measured with an oscilloscope with 1 MΩ input resistance

### Sample& Hold Circuit

Fig. 3 shows a simple S/H circuit consisting of a switching FET M1, a hold capacitor \( C_h \), and an output buffer (transistors M2, M3), where the analog input signal is held as a certain amount of charges when M1 is turned off. For high speed S/H performance a very high transconductance transistor is needed which perfectly fits to the performance of InAs NW MISFET [2]. Therefore, the transistor M1 is an InAs NW MISFET. On the other hand a high current driver is required which has been realized by conventional InP heterojunction MISFETs again by heterogeneous integration. Fig. 2c shows the input and output waveforms experimentally obtained from the circuit shown in Fig. 2b which confirms the basic sample-and-hold circuit operation. The observed offsets at the transition from the track mode to the hold mode are due to the clock feed through which can be suppressed by a novel differential scheme S/H circuit enabling 7 bit resolution up to almost 1 GHz sampling frequency [3].
Summary

A novel heterogeneous integration scheme for heterogeneous nanowire transistor implementation in existing circuits is proposed. Both an inverter circuit and a sample & hold circuit function is experimentally confirmed. A combination of InAs nanowire transistor with InP-based heterojunction MISFET is used to form sample & hold circuits at 100 MHz sampling frequency. These data outperform existing nanowire circuits and underline the potential of this approach.

Fig. 3. Sample & hold Circuit: (a) schematic, (b) SEM micrograph, and (c) input and output waveforms obtained experimentally at 100 MHz sampling frequency
Acknowledgment

This work is supported from JST-DFG Programme on Nanoelectronics, project “Nanowire/CMOS Heterogeneous Integration for Next-Generation Communication Systems”.

References:

