OUTLINE

Introduction

Total Dose Effects in thin gate oxides

RILC, RSB, SEGR, Latent Damage

Microdose Effects

Device Scaling

- Bulk & SOI FinFETs
- Ge devices

Conclusions
INTRODUCTION

COTS important for Space Applications

Advanced CMOS Technologies

Reduced Gate Dielectrics

Alternative Substrates: SOI, sSOI, Ge, sGe, GOI...

Advanced Process Modules:

  High-κ Dielectrics, Strain Engineering, ...

Alternative Device Concepts

  Double gate, FinFETs, GAA, Nanowires, ...

Impact on Radiation Hardening?
INTRODUCTION

**Ionizing Damage:** creation of electron-hole pairs across the band gap

- Linear Energy Transfer (LET) function (in MeV cm$^2$/g)
- 1 rad$=100$ erg/g$=6.24 \times 10^{13}$ eV/g - 1 Gray$=1$ J/kg$=100$ rad

**Displacement Damage:** creation of vacancy-interstitial (V-I) pairs by displacement of a lattice atom

- Non Ionizing Energy Loss (NIEL) function
The energy loss rate through ionization and excitation of the Si lattice (LET) and through atomic displacements (NIEL) versus proton energy. Only a fraction of 1% of the energy loss goes into displacement processes.
IONIZING DAMAGE IN MOS

Gate: carries away the charge

Silicon: electron-hole pairs can recombine in the neutral bulk

In case of a p-n junction, the electric field separates electrons and holes. This leads to a transient charging phenomenon

→ Single Event Upsets (SEU)

Permanent ionizing damage only in the dielectric layers: gate oxide, isolation or field oxide and buried oxide (SOI)
STANDARD TOTAL DOSE RADIATION EFFECTS

(1) Electron-hole pairs generated by ionizing radiation

(2) Hopping transport of holes through localized states in SiO₂ bulk

(3) Deep hole trapping near Si/SiO₂ interface

(4) Radiation-induced interface traps within Si bandgap

\( N_{ot} \) & \( N_{it} \)
GATE OXIDE SCALING

Gate current before (full lines) and after (dashed lines) a 67 MeV $2.9 \times 10^{12}$ p/cm$^2$ proton irradiation for a 0.09 $\mu$m n- and 0.08 $\mu$m p-MOSFET with 2.0 nm oxide.
DEVICE SCALING

\[ \Delta V_t \sim t_{ox}^2 \]

Good TID resistance of the Gate oxide

Radiation effects will be caused by parasitic conduction related to

- Shallow Trench Isolation oxide: Bulk
- Buried oxide for SOI devices

Occurrence of other radiation related phenomena
IONIZING DAMAGE: THIN GATE OXIDES

Uniform gate current flow

Breakdown path

Trap-assisted RILC

RILC by radiation-induced Neutral electron traps
IMPACT OF HIGH-ENERGY IONS ON GATE OXIDE

Radiation-Induced Leakage Current (RILC)

Radiation-Induced Soft Breakdown (RSB)

Increase of off-state power consumption but no real concern
ION-INDUCED DEGRADATION OF GATE DIELECTRICS

SINGLE EVENT GATE RUPTURE


**SEGR**

* Operating voltage lower than critical value

* Critical LET threshold
LATENT RADIATION DAMAGE IN THIN GATE OXIDES


* No parameter shift after irradiation only
* Reduced oxide lifetime after accelerated testing

Let thermal annealing:

Weibull lifetime distribution of MOS capacitors subjected to constant voltage stress at $V_{\text{stress}} = -4.9$ V before and after heavy ion irradiation

LET > 30 MeV/cm²
LATENT RADIATION DAMAGE IN THIN GATE OXIDES


Weibull lifetime distribution of MOS capacitors subjected to constant voltage stress at $V_{\text{stress}}=-5.0$ V before and after $^{60}$Co irradiation.
LATENT RADIATION DAMAGE - ION FLUENCE EFFECT


Gate current during CVS at $V_{CVS} = 4.2$ V on three samples with gate area $10^{-2}$ cm$^2$ irradiated with 256-MeV I ions at different fluences

Excess gate current Density ($J_e$) normalized to the ion fluence ($\phi$) measured during CVS at $V_{CVS}=4.2$ V
LATENT RADIATION DAMAGE – STRESSING VOLTAGE


\[
\langle \Delta I(t_s) \rangle = \Delta I N [1 - \exp(-\lambda t_s)]
\]

Gate current derivative \(dI_g/dt\) of the gate current, equivalent to the density of spots, with respect to the stressing time during CVS. The derivative has been evaluated as the slope of the initial part of the gate current evolution \(t_{stress} < 1000 \text{ s}\), i.e., where the gate current increases almost linearly.
Gate current measured at $V_g = V_{g,\text{stress}}$ during FN injection of devices processed in an 0.1 $\mu$m PD SOI technology. $V_{g,\text{stress}}$ starts from 2.5 V and increases up to 4 V with 50-mV step every 100 s. The stress was performed on fresh and irradiated devices with two different ion fluences (2.5 and 0.5 I ions/$\mu$m$^2$).
65 NM FD SOI TECHNOLOGY
NO CHANGE.


Gate current time to breakdown for irradiated (2.5 I ions/µm²) and unirradiated FD SOI MOSFETs (W=L = 10 µm/10 µm) fabricated in a 65 nm technology with different strain levels. The devices were stressed with a staircase voltage from 2 V to 4 V with 50-mV steps, each lasting 100 s.
HEAVY ION STRIKES: MICRODOSE EFFECTS


Defect generation in the oxide

Statistical in nature

charge build-up in the LDD region

charge build-up in the STI
TRANSISTOR SCALING

New process modules
New materials
New device concepts

Front End

90-65-45
Strain, USJ

45-32
High-k, Metal Gate

32-22-16
Non-planar devices

16 and beyond

High-k, Metal Gate

New process modules
New materials
New device concepts
BULK AND SOI FINFETS


I_d and g_m as a function of V_g for a SOI (a) and a bulk p-MuGFET (b). Both devices have a single fin and a fin width of 885 nm. (L=165 nm, V_d=-50mV).

60Co irradiation of 10 hours at a dose rate of 1 kGy/hr.
HIGH MOBILITY SUBSTRATES
Ge DEVICES

CONCLUSIONS

- Deep submicron CMOS technologies are radiation hard for total dose effects
  - STI or BOX must be optimized

- RILC, RSB, SEGR and Latent Damage

- For thin gate oxides heavy ion strikes are important

- Microdose effects have to be taken into account requiring a statistical analysis of a technology

- New process modules, new materials and alternative device concepts have to be investigated
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