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EDS Chapter Germany Meetings

Munich, March 13, 2018

Modeling of Systems and Parameter Extraction Working Group

(Arbeitskreis Modellierung von Systemen und Parameterextraktion)

Location: Infineon Technologies AG, Neubiberg, Germany

Summary:

The MOS-AK Compact Modeling Association, a global compact/SPICE modeling and Verilog-A standardization forum, held its Spring compact/SPICE workshop in Munich.

The event was hosted on March 13, 2018, by Infineon Technologies AG in Neubiberg.

The technical program of the event was coordination by Klaus-Willi Pieper, Infineon, and the MOS-AK TPC Committee. The workshop has received full industrial sponsorship by Infineon Technologies AG (lead sponsor) with technical program promotion provided by ASCENT Network [3], Keysight Technologies [4], IJHSES [5] as well as NEEDS [6] of nanoHUB.org [7].

The MOS-AK workshop was opened by Klaus-Willi Pieper, Principal Compact Modeling Smart Power Devices at Infineon, who has welcomed all the attendees and shared Infineon view on the compact modeling and its importance in the TCAD/EDA modeling/design ecosystem.

A group of 40+ international academic researchers and modeling engineers attended 10 technical compact modeling presentations covering full development chain from the nanoscaled technologies thru semiconductor devices modeling to advanced IC design support. The MOS-AK speakers have shared their latest perspectives on compact/SPICE modeling and Verilog-A standardization in the dynamically evolving semiconductor industry and academic R&D. The event featured advanced technical presentations covering compact model development, implementation, deployment and standardization covering full engineering R&D chain:

- TCAD/processing,
- device modeling,
- transistor level IC design support.

These contributions were delivered by leading academic and industrial experts, including:

[1] Klaus-Willi Pieper, Overview of the Compact Modeling at Infineon [8];

[2] James Ma et al, Advanced Fast on-wafer Low-frequency Noise Measurement with High Resolution, Wide Bandwidth and Large Biasing Current Range [9];

[3] Volker Gloeckel, Advances in Statistical Compact Modeling [10];

[4] Markus Becherer, et al, Compact Modeling of Nanomagnetic Logic Devices and Circuits [11];

[5] Gražvydas Žiemys, Devices for Nanomagnetic Logic [12];

[6] Paul Roseingrave, Modelling Emerging Devices through EU ASCENT Network [13];

[7] Jushan Xie, How Is CMC Standard Model Implemented and Verified In Simulator? [14];

[8] Maria Cotorogea et al, Virtual Prototyping for Power Diode and IGBT Development [15];

[9] Franz Sischka, et al, Modeling of Device Aging - Example: Diode [16];

[10] Katja Puschkarsky, Device Aging Simulations Enabling Circuit Optimizations [17];

[11] Fabio A. Velarde Gonzalez, Integration of Aging Models Across Different EDA Environments A case study implementing HCI and NBTI models for X-FAB XU035 CMOS technology [2];

During complementary MOS-AK Panel Discussion on Compact Model Licensing Peter Lee, CMC Chair highlighted current status of the CMC compact model licensing status, stating that final discussions are converging to establish official licensing in the next few months. All the presentations are available online for download at <http://www.mos-ak.org/munich_2018>.

Selected best presentation will be recommended for further publication in the IJHSES [5].